Archit Gupta

Personal Data

275 Li Ka Shing Center University of California Berkeley, CA 94704 +1 (510) 833 8411 architgupta@berkeley.edu http://www.eecs.berkeley.edu/~architgupta https://github.com/architgupta93

EDUCATION

May 2018 -Present	University of California, Berkeley, CAPhD candidate, EECS DepartmentAdvisors - David Foster, Jose Carmena	Gpa: 3.87/4.0
August 2015 -May 2018	University of California , Berkeley, CA MS, EECS Department Advisor - Jaijeet Roychowdhury	Gpa: 3.85/4.0
July 2011 -April 2015	Indian Institute of Technology , Mumbai, India B.Tech (Honors) in Electrical Engineering Minor: Computer Science and Engineering	Gpa: 9.55/10.0

PUBLICATIONS

[1] A. Gupta. Table-based device modeling: Methods and applications. 2018.

- [2] A. Gupta, A. G. Mahmutoglu, and J. Roychowdhury. A-LA-CARTE: A LAgrange interpolant using Chebyshev sampling for Accurately Representing Table modEls. In *TECHCON*, 2017.
- [3] A. Gupta, T. Wang, A. G. Mahmutoglu, and J. Roychowdhury. STEAM: Spline-based tables for efficient and accurate device modelling. In 2017 22nd Asia and South Pacific Design Automation Conference (ASP-DAC), pages 463–468. IEEE, 2017.
- [4] K. Kumar, A. Gupta, R. Shah, A. Karandikar, and P. Chaporkar. On analyzing indian cellular traffic characteristics for energy efficient network operation. In 2015 Twenty First National Conference on Communications (NCC), pages 1–6. IEEE.
- [5] A. G. Mahmutoglu, T. Wang, A. Gupta, and J. Roychowdhury. Well-posed device models for electrical circuit simulation, 2017.

RESEARCH

Understanding the role of hippocampal sequences in spatial planning and memory.

Advisors: David Foster, Jose Carmena [DOCTORAL THESIS]

We study spontaneous reactivation of sequences in the hippocampus. Employing fast real-time decoding from hundreds of simultaneously recorded cells and electrical/optogenetic manipulation allows us to establish causal relationships between different types of sequences observed in the hippocampus and behavior.

In-vivo, closed loop targeting of Hippocampal pyramidal cells.

Hippocampus consists of a thin layer ($\sim 40 - 100\mu m$ in a rat) of pyramidal cells that are believed to play a significant role in memory formation and spatial navigation. It is also one of the most widely studied brain regions. Targeting this cell layer is technically difficult, often requiring years of experience in electrophysiology and hundreds of human hours for each individual subject. We are working on a closed loop methodology to target cells in the Hippocampus by using electrical feedback from the recording electrodes to navigate the brain.

Table-based device modeling - Methods and Applications

Advisor: Jaijeet Roychowdhury [MS THESIS]

As semiconductor devices shrink, physics-based models have to be refined with empirical parameters and equations to account for newly observed phenomenon. This eventually slows down these models, often pushing circuit simulation times to weeks and months even for modest designs. We proposed polynomial interpolation techniques to bridge the gap between realistic physics-based models and fast circuit simulation. In [1, 3], we demonstrate how multidimensional splines and Chebyshev interpolants can be used to accelerate circuit simulation without losing the modeling accuracy that physics-based models offer.

Posters & Presentations

A. Gupta, J. Roychowdhury. ABCD-CPS: Accurate Booleanization of Continuous Dynamics for Cyber-Physical systems, AMS Design Automation Workshop, ICCAD 2017.

ACADEMIC SERVICES

[2018-PRESENT] Reviewer, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.

WORK EXPERIENCE

May -	SOC Design and Optimization at SAMSUNG DMC RND CENTER, Suwon				
June 2014	South Korea — Guide: Dr. Dongjin Lee				
	Designed a controller for Samsung's Temperature Sensing analog IP. Integrated and synthesized the controller along with other peripherals into an SoC. Developed a glitch free mechanishm to switch clocks using Clock Gating Cells. Optimized the design for power consumption (im- proving gating efficiency) and empirically evaluated the energy complexity of algorithms on the aforementioned SoC			l synthesized mechanishm imption (im- ithms on the	
	Teaching Assistant at Indian Institute of Technology, Bombay				
Jan 2013 -	MA 106	Linear Algebra	Prof. Neela Natraj	Jan - Mar 2013	
May 2014	MA 108	Differential Equations	Prof. U. K. Anandvardhanan	Mar - May 2013	
	MA 106	Linear Algebra	Prof. Murali K. Srinivasan	Jan - Mar 2014	

Awards & Achievements

• Recepient of Ansellmo J. Macci fellowship at UC Berkeley	2015-16
• Awarded the Best Internship Project at Samsung Global Research HQ for SoC design and optimization, suwon, South Korea	June 2014
• Indian delegate at the annual Winter School organized by the Institute of Theoritical Computer Science and Communications, CUHK, HONG KONG	Jan 2014
• Gold Medalist at Indian National Physics Olympiads (INPhO) and Indian National Chemistry Olympiads (INChO). Qualified for Orientation Cum Selection Camp for the International Physics and Chemistry olympiads (IChO, IPhO), held at BARC, India	July 2011
• Secured All India Rank 14 in the Joint Entrance Examination for Indian Institutes of Technology (IIT-JEE). Ranked 1st in Kanpur Zone	Apr 2011
• All India Rank 3 in the National Science Olympiads and All India Rank 4 in the International Mathematics Olympiads organized by Science Olympiad Foundation	Mar 2010
• Felicitated by former President of India, Dr. A. P. J. Abdul Kalam for excellence in Academics at Rashtriya Indian Military College, Dehradun, India	Apr 2009

EXTRA-CURRICULAR ACTIVITIES

- Silver Medalist in Hockey at Inter IIT Sports Meet held at IIT Kharagpur (Dec 2012).
- Awarded Institute Special Mention, for contribution to sports at IIT Bombay in 2012-2013
- Institute Hockey Secretary (2013-14): Member of the Institute Sports Council at IIT Bombay. Organized and conducted Inter-Hostel hockey championships, trials and selection of Institute teams, acquiring and managing equipment and infrastructure.